REMARKS

The Examiner's Office Action mailed on March 1, 2004 has been received and its contents carefully considered.

In the Action, the title of the invention is objected to as not being adequately descriptive of the invention to which the claims are directed. The title is amended herein to read "MANUFACTURING METHOD FOR SEMICONDUCTOR DEVICE HAVING A T-TYPE GATE ELECTRODE." Approval of the amended title and withdrawal of the objection are respectfully requested.

Claims 1-20 are pending in this application. Claims 2, 6, 13 and 15 are canceled without prejudice or waiver, and claims 1 and 12 are amended herein. Claims 1 and 12 remain the independent claims.

In the present Action, the Examiner has rejected claims 1-3 and 5-20 under 35 USC 102(b) as being anticipated by Wu (U.S. Patent No. 6,239,007 B1). Independent claims 1 and 12 are amended herein by incorporating the limitations of claims 2 and 6, and 13 and 15, respectively to more clearly distinguish over the applied Wu reference.

The Examiner points to Wu as disclosing all of the elements recited in claim 1. Specifically, the Examiner asserts that Figures 1A-1F of Wu and the related text, disclose: forming first polysilicon 102 serving as a gate on a semiconductor substrate 100; forming a first insulating film on the semiconductor substrate to cover the first polysilicon; forming a second insulating film 106 on the first insulating film; selectively etching the second insulating film until the first insulating film located on an upper surface of the gate is exposed (Figure 1B); selectively etching the first insulating film located on the upper surface of said gate until the upper surface of said gate is exposed (Figure 1C); burying a space in which the first insulating film is etched, and forming a second polysilicon 108 on the second insulating film Figure 1D); etching the second polysilicon, exposing the second insulating film, and leaving the second polysilicon in the space (Figure 1E); etching the second insulating film (Figure 1F); etching the first insulating film (Figure 1F); forming high melting point metal covering the second polysilicon; siliciding the second polysilicon by a heat treatment (column 3, lines 35-50); and removing unreacted high melting point metal (Figure 1F).

The Applicant respectfully disagrees. Column 1, line 64 through column 2, line 9, summarizes the process disclosed in Wu as follows:

> "In the present invention, two insulation layers, each having a different etching rate, are sequentially formed over a conventional gate structure. A planarization of one of the insulation layers is next carried out. Utilizing the difference in etching rate between the insulation layers, the insulation layer above the gate structure is removed to expose the gate structure. A conductive layer is formed over the exposed gate structure. Another planarization is carried out so that only the portion of the conductive layer above the gate structure is retained. While using the conductive layer above the gate structure as an etching mask, the two insulation layers are removed. Finally, a silicide process is carried out to form a silicide layer of the conductive layer." (Emphasis added.)

Wu further explains that "[t]he planarization of the insulation layer 106 [i.e., the second insulation] can be carried out, for example, by chemical-mechanical polishing (CMP)," and also that "[t]he conductive layer 108 above the insulation layer 106 can be removed, for example, by chemical-mechanical polishing while using the insulation layer 106 as a polishing stop layer." In the claimed invention, by contrast, removal of the second insulating film in order to expose the first insulating film located on the upper surface of the gate, is carried out by etching back using a dry etching method (see application page 7, lines 8-9). Likewise, in the later step where the second polysilicon is removed from the second insulating film, leaving the second polysilicon in the space formed over the upper surface of the gate, the process is carried out by etching back using a dry etching method (see application page 7, lines 25-27). The etching processes used in the present invention are significantly different from and far simpler than the chemical-mechanical polishing steps taught by Wu, resulting in a method that is faster and less expensive than the prior art.

In order to more fully reflect the distinguishing features of the claimed invention, claims 2 and 6 are canceled and claim 1 is amended herein to incorporate their limitations. It is respectfully submitted that amended claim 1, as well claims 3-5 and 7-11, patentably distinguish over the applied prior art.

In the Action, independent claim 12 is rejected for much the same reasons as claim 1. Claim 12 is amended herein to incorporate the limitations of canceled claims 13 and 15. For the reasons discussed above, it is respectfully submitted that amended claim 12, as well claims 14 and 16-20, patentably distinguish over the Wu reference.

Claim 4 stands rejected under 35 USC 103(a) as being obvious over Wu. The rejection is respectfully traversed.

The Examiner acknowledges that Wu fails to disclose that limitation of claim 4 "wherein said first insulating film is formed to be thicker than said first polysilicon." The Examiner argues that it would have been obvious to one of ordinary skill in the art at the time the invention was made, to form the first insulating film to be thicker than the first polysilicon, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art.

The Applicant respectfully disagrees. The limitation of claim 4 represents a difference in kind rather than degree. Figures 1A-1E in Wu all clearly disclose that insulation layer 104 is thinner than the height of gate structure 102. There is nothing in either the figures or text of Wu to suggest the claimed limitation. Moreover, contrary to the Examiner's assertions, the claimed limitation has advantages that are not obvious from the prior art. The present application discloses two exemplary embodiments - the first in which the first insulating film is formed to be thinner than the first polysilicon, as in the prior art, and the second in which the first insulating film is formed to be thicker than the first polysilicon. The second embodiment advantageously overcomes certain processing irregularities to which the first is prone, ensuring more reliable results (see application page 11, lines 8-27). Neither the deficiency in the first embodiment nor the improvement resulting from the limitation of claim 4 are suggested by the prior art. Hence, it is respectfully submitted that claim 4 patentably distinguishes over the applied Wu reference.

The Examiner's various objections and rejections having been fully addressed, it is submitted that the application is in condition for allowance. Notice of such, with claims 1, 3-5, 7-12, 14 and 16-20, is earnestly solicited.

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Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,

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Date

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